REMARKS

Claims 1-27 are rejected under 35 USC §112, first paragraph, as not being supported by the application as filed.

The Examiner's rejections are respectfully traversed.

It is respectfully submitted that the subject matter claimed in claim 1 is described in the specification, and furthermore, is described in such a way as to reasonably convey to one skilled in the relevant art that the inventors at the time the Application was filed had possession of the invention as claimed.

The invention claimed in claim 1 is directed towards a method for forming a semiconductor device comprising first, second and third layers with a component being formed in the second layer and with first and second etch stop layers located between the first and second layers, and the second and third layers, respectively. Claim 1 requires that the second etch stop layer is to be bonded to one of the second and third layers, and that prior to bonding of the second etch stop layer to the one of the second and third layers the second etch stop layer is to be patterned to define the component in the second layer.

In the description of the preferred embodiment of the invention, which is given with reference to Figs. 1 to 11, the first layer is referred to as the lower layer 4, the second layer is referred to as the intermediate layer 5 and the third layer is referred to as the upper layer 6, all three layers being of single crystal silicon. The first and second etch stop layers are identified as the first etch stop layer 8 and the second etch stop layer 9, respectively. The first etch stop layer 8 is described as being located between the lower layer 4 and the intermediate layer 5, while the second etch stop layer 9 is described as being located between the intermediate layer 5 and the upper layer 6.

The first and second etch stop layers 8 and 9 are both described as being oxide

layers which are thermally grown layers. The first etch stop layer is grown on the lower layer 4 and bonded to the intermediate layer 5. Additionally, in the description of the preferred embodiment of the invention the second etch stop layer 9 is described as being thermally grown on the intermediate layer 5 and bonded to the upper layer 6. Prior to bonding of the second etch stop layer 9 to the upper layer 6, the second etch stop layer 9 is patterned to define micro-mirrors 10 which are to be subsequently etched in the intermediate layer 5 through the upper layer 6 after the three layers 4, 5 and 6 have been assembled together.

Patterning of the second etch stop layer 9 prior to bonding to the upper layer 6 permits etching of the component in the intermediate layer 5 through the upper layer 6. The essence of the invention is the provision of a second etch stop layer 9 between the intermediate layer 5 and the upper layer 6 which is patterned prior to it being finally located between the intermediate layer 5 and the upper layer 6. Accordingly, how the second etch stop layer 9 is formed and finally located between the intermediate and upper layers 5 and 6 is not critical to the invention, once the second etch stop layer 9 is patterned prior to being finally located between the intermediate and upper layers 5 and 6. It is respectfully submitted that this is clearly taught in the specification.

As discussed, in the description of the preferred embodiment of the invention the second etch stop layer 9 is described as being grown on the intermediate layer 5 and bonded to the upper layer 6. Under the heading "Summary of the Invention" from page 2, line 29 to page 3, line 8, the invention is clearly stated as being "a method for forming a semiconductor device comprising first, second and third layers, with a component being formed in the second layer, and first and second etch stop layers being located between the first and second layers, and the second and third layers, respectively". Thus, from this

statement it is clear that the second etch stop layer is to be located between the second (intermediate) and third (upper) layers. It is further stated at page 2, line 33 "the second etch stop layer being bonded to one of the second and third layers". In other words, the second etch stop layer is to be bonded to either the second (intermediate) layer or the third (upper) layer.

The method comprises three steps that are set out at page 3, line 2 to line 8. The first step is set out at lines 2 to 4 as being:

"prior to bonding the one of the second and third layers to the second etch stop layer, patterning the second etch stop layer to define the component in the second layer for facilitating etching of the second layer through the third layer".

As will be appreciated by those skilled in the art to whom the specification is addressed, an etch stop layer is not a self-supporting layer, and thus must be formed on a silicon or other such semiconductor layer. Furthermore, where an etch stop layer is a buried layer between two layers, as is the case in the semiconductor device of the present invention, the etch stop layer must be formed on one of the layers, and bonded to the other layer. This will be well known and understood by those skilled in the art to whom the specification is addressed. Therefore, since as stated in the specification at page 2, line 29 to page 3, line 8 the second etch stop layer is to be located between the second and third layers, and is to be bonded to one of the second and third layers, the etch stop layer must be formed on the other one of the second and third layers to which it is not bonded.

In the preferred embodiment of the invention, the second etch stop layer 9 is described as being formed on the second (intermediate) layer 5, and bonded to the third (upper) layer 6. Therefore, from the summary of the invention appearing at page 2, line 29 to page 3, line 8, it would be perfectly evident to a person of ordinary skill in the art to

whom the specification is addressed that the inventors envisaged at the date of filing the Application that the second etch stop layer 9 in certain cases would instead of being formed on the second (intermediate) layer 5 be formed on the third (upper) layer 6 and be bonded to the second (intermediate) layer 5. The patterning would take place prior to bonding of the second etch stop layer 9 to the second (intermediate) layer 5, as it does in the preferred embodiment prior to bonding of the second etch stop layer 9 to the third (upper) layer 6.

Accordingly, it is respectfully submitted that Applicants clearly had possession of the invention as claimed in claim 1 at the time the application was filed.

Applicants have summarized the invention from page 2, line 29 to page 8, line 11, and in particular, from page 2, line 29 to page 3, line 8. In addition, Applicants have described with reference to Figs. 1 to 11 the best method known to them for carrying out the invention. In summarizing the invention from page 2, line 29 to page 8, line 11, and in particular from page 2, line 29 to page 3, line 8, and by describing the best method for carrying out the invention known to them, it is respectfully submitted that the Applicants have clearly shown that they were in possession of the invention at the time the application was filed. This is particularly so when the summary of the invention at page 2, line 29 to page 3, line 8 is read in conjunction with the description of the preferred embodiment described with reference to Figs. 1 to 11.

While it is incumbent on the Applicants to describe the best method known to them for carrying out the invention, it is respectfully submitted that the Applicants are not obliged to describe every single possible method of carrying out the invention.

Accordingly, it is respectfully submitted that the Applicants have described the invention in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors at the time the application was filed had possession of the

claimed invention.

In view of the above, it is respectfully submitted that claim 1 should be allowable and allowance is respectfully requested.

Once the Examiner is satisfied of the allowability of claim 1, it is respectfully submitted that since Claims 2 to 27 are dependent either directly or indirectly on claim 1, the remaining Claims 2 to 27 should likewise be allowable, and allowance is respectfully requested.

Claims 28-39 are indicated as being allowable.

In view of the foregoing comments, Applicants contend that all of the claims are now in full compliance with 35 USC §112. Accordingly, Applicants submit that all of the claims should now be in condition for allowance, and an early indication of same is respectfully requested.

Applicants' undersigned representative would like to suggest that a telephonic interview be held in order to expedite the prosecution of the application, and to avoid a possible appeal to the issues related to 35 USC §112.

Respectfully submitted,

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